IN THE CLAIMS:

1.-14. (Canceled)

15. (Original) A method, comprising:

commonly connecting source and drain regions of a plurality of transistor elements to a first electric potential by a first contact pad;

commonly connecting gate electrodes of said plurality of transistor elements to a second electric potential by a second contact pad;

connecting a common well region of said plurality of transistor elements to a third electric potential by a third contact pad; and

assessing a reliability of gate insulation layers of said plurality of transistor elements by monitoring a gate leakage current of said plurality of transistor elements.

16. (Original) A method, comprising:

commonly connecting source and drain regions and a gate electrode of at least one N-channel transistor structure and at least one P-channel transistor structure to a first electric potential by a first contact pad;

connecting a P-well region of said at least one N-channel transistor structure to a second electric potential by a second contact pad;

connecting an N-well region of said at least one P-channel transistor structure to a third electric potential by a third contact pad; and

assessing a reliability of gate insulation layers of said at least one N-channel transistor structure and said at least one P-channel transistor structure by determining a failure event.

17. (Original) The method of claim 16, wherein said second and third potentials are of opposite polarities.

18. (Original) The method of claim 17, wherein said second and third potentials are applied substantially simultaneously.

19. (Original) The method of claim 17, wherein said second and third potentials are applied sequentially.

20. (Original) The method of claim 19, wherein said second and third potentials are applied as pulses in an alternating manner.

21. (Original) The method of claim 16, wherein said failure event is determined by detecting abrupt changes of a signal indicative of a dielectric breakdown of a gate insulation layer of said at least one N-channel transistor structure and said at least one P-channel transistor structure.

22. (Original) The method of claim 21, wherein said signal represents a leakage current through said gate insulation layers.

23. (Canceled)